

Patent Claims

1. A master latch circuit with signal level
5 displacement for a flip flop which is clocked by a
clock signal (Clk), the master latch circuit (10)
having:

10 (a) a signal delay circuit (13), which delays the clock
signal (Clk) present with a specific time delay (ΔT);
and

15 (b) a circuit node (14) which, in a charging phase, in
which the clock signal (Clk) present is logically low,
is charged to an operating voltage (V_B) and which, in an
evaluation phase, if the clock signal (Clk) present and
the delayed clock signal (Clk_{DELAY}) are logically high,
can be discharged depending on a data signal (D)
present,

20 (c) the circuit node (14) being connected to a
reference potential via at least one capacitor (15).

2. The master latch circuit as claimed in claim 1,
characterized

25 in that the circuit node (14) is discharged in the
evaluation phase if the data signal (D) present is
logically high,

and in that the circuit node (14) is not discharged in
the evaluation phase if the data signal (D) present is
logically low.

30 3. The master latch circuit as claimed in claim 1,
characterized in that the circuit node (14) is
connected to an input of a first isolating circuit (12)
clocked by the clock signal (Clk).

35 4. The master latch circuit as claimed in claim 3,
characterized

in that the first isolating circuit (12) has an output

connected to a slave latch circuit (11), which buffer-stores the output signal of the master latch circuit (10).

5 5. The master latch circuit as claimed in claim 4,
characterized
in that an inverter (18) is connected downstream of the
slave latch circuit (11).

10 6. The master latch circuit as claimed in claims 3 to
5,
characterized
in that the output of the first isolating circuit (12)
is fed back to the input of the first isolating circuit
15 (12) via a second clocked isolating circuit (29), the
second isolating circuit (29) being clocked with the
delayed clock signal ($\text{Clk}_{\text{DELAY}}$).

20 7. The master latch circuit as claimed in claim 1,
characterized
in that the master latch circuit (10) has a first
controllable switch (19), which is driven by the
inverted clock signal ($\overline{\text{Clk}}$) and which switches the
operating voltage (V_B) present to the circuit node (14)
25 if the clock signal (Clk) is logically low.

8. The master latch circuit as claimed in claim 7,
characterized
in that the first controllable switch (19) is a PMOS
30 transistor.

9. The master latch circuit as claimed in claim 1,
characterized
in that the master latch circuit (10) has
35 a second controllable switch (24),
a third controllable switch (26), and
a fourth controllable switch (28),

which are connected in series with one another between the circuit node (14) and the reference potential (GND).

- 5 10. The master latch circuit as claimed in claim 9, characterized in that the second controllable switch (24) is driven by the delayed inverted clock signal (\overline{Clk}_{DELAY}).
- 10 11. The master latch circuit as claimed in claim 9, characterized in that the third controllable switch (26) is driven by the data signal (D) present.
- 15 12. The master latch circuit as claimed in claim 9, characterized in that the fourth controllable switch (28) is driven by the clock signal (Clk).
- 20 13. The master latch circuit as claimed in claims 10 to 12, characterized in that the second, third and fourth switches (24, 26, 28) are NMOS transistors.
- 25 14. The master latch circuit as claimed in claim 9, characterized in that the capacitor (15) is connected in parallel with the second, third and fourth switches (24, 26, 28).
- 30 15. The master latch circuit as claimed in claim 1, characterized in that the time delay (ΔT) of the signal delay circuit (13) is adjustable.
- 35 16. The master latch circuit as claimed in claim 14,

characterized

in that the time constant (τ) with which the capacitor (15) is discharged via the series-connected switches (24, 26, 28) during the evaluation phase if the data signal (D) present is logically high is less than the time delay (ΔT) of the signal delay circuit ($\tau \ll \Delta T$).
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17. The master latch circuit as claimed in claim 1, characterized

10 in that the time delay (ΔT) of the signal delay circuit (13) is less than the time period of the clock signal (Clk) ($\Delta T \ll T_{Clk}$).

15 18. The master latch circuit as claimed in claim 1, characterized

in that the signal delay circuit (13) is formed by a plurality of inverter stages connected in series.

20 19. The master latch circuit as claimed in claim 1, characterized

in that the data signal (D) drives controllable switches (24, 26, 28) that are transistors of the same type (NMOS; PMOS).

25 20. The master latch circuit as claimed in claim 1, characterized

in that the master latch circuit (10) has only a single supply voltage.

30 21. The master latch circuit as claimed in claim 1, characterized

in that the capacitance of the capacitor (15) is programmable.

35 22. The use of a master latch circuit (10) as claimed in claim 1 for an edge triggered flip flop (1) with a slave latch circuit (11) for buffer-storing the output

signal of the master latch circuit (10) and with a clocked isolating circuit (12) for isolating the master latch circuit (10) from the slave latch circuit (11).